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| 10/650,325 | 08/27/2003 | Jaime Bayan | NSC1P274/P05649 | 6886 |

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| EXAMINER | |
|---|---|
| IM, JUNGHWA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/650,325 | BAYAN ET AL. | |
| | Examiner | Art Unit | |
| | Junghwa M. Im | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *10 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Inventorship*

In view of the papers filed August 19, 2004, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship by Mostafazadeh et al. The Applicant is advised to make an appropriate correction.

### *Election/Restrictions*

Applicant's election of claims 1-23 in the reply filed on August 19, 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 11 and 15 recite a limitation of " ... wire bonding landings exposed on a top surface ..." This limitation recites what is shown in Fig. 4B and /or Fig. 5A, and it is pointed that what is shown in Fig. 4B and 5A is an intermediate structure. As disclosed in paragraph [0020], Fig. 4B and 5A are a structure before encapsulation. Therefore, after encapsulation as

disclosed in paragraph [0028], the wire bonding landings are *not exposed*, rather they are encapsulated/covered with molding material. Further confusing matter is that claim 15 recites a limitation of "a second dielectric layer that encapsulates the die and the plurality of connectors" and the instant invention does not disclose this limitation. In detail, the instant invention does not disclose that the top surface of the wire bonding landings is exposed while the die and the plurality of connectors are encapsulated.

Claims 1, 11 and 15 include a limitation which implies as if a wire bonding landings and the lead segments are distinctively different portions of the structure. In particular, claim 11 recites a limitation of "...wherein at least some of the wire bonding landings are thinner than the substrate panel, such that the thinner wire bonding landings are not exposed on the bottom surface of the substrate panel, and at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel" implying two distinctive structures. However, the figures of the instant invention explicitly disclose that the wire bonding landing is a portion of the lead segment.

Claims 2-10, 12-14 and 16-23 are dependent on the rejected base claim.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 7, 9, 11-12, 14-15, 17, 19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang (US 6384472).

Regarding claim 1, insofar as understood, Fig. 5 of Huang shows a substrate panel [Fig.10] for use in semiconductor packaging, comprising:

a lead-frame panel [602 in Fig. 10], including ail array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel, a plurality of wire bonding landings [106] exposed on a top surface of the substrate panel, and lead segments [104] electrically coupling selected wire bonding landings to associated contacts [col. 4, lines 31-32]; and

a dielectric material [124] that fills spaces [122] between adjacent lead segments [col. 3, lines 54-56]

Regarding claim 2, Fig. 5 of Huang shows a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and the bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts.

Regarding claim 4, Fig. 5 of Huang shows at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

Regarding claim 5, Fig. 10 of Huang shows the device areas are arranged in at least one two dimensional array.

Regarding claim 7, Fig. 5 of Huang shows each device area further includes a die attach pad [102], the die attach pad being exposed on the top surface of the substrate panel.

Regarding claim 9, it is inherent that at least one of the wire bonding landings is electrically coupled to the die attach pad since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

Regarding claim 11, insofar as understood, Fig. 5 of Huang shows a substrate panel [Fig. 10] for use in semiconductor packaging, comprising:

a lead-frame [602 in Fig. 10] panel including a two dimensional array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel, a plurality of wire bonding landings [106] exposed on a top surface of the substrate panel, and lead segments [104] electrically coupling selected wire bonding landings to associated contacts [col. 4, lines 31-32]; and

a dielectric material [124] that fills spaces [122] between adjacent lead segments, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and a bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts; and

wherein at least some of the wire bonding landings are thinner than the substrate panel, such that the thinner wire bonding landings are not exposed on the bottom surface of the substrate panel, and at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

Regarding claim 12, Fig. 5 of Huang shows each device area further includes a die attach pad [102], the die attach pad being exposed on the top surface of the substrate panel.

Regarding claim 14, it is inherent that at least one of the wire bonding landings is electrically coupled to the die attach pad since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

Regarding claim 15, insofar as understood, Fig. 5 of Huang shows a packaged integrated circuit, comprising:

a substrate [600 in Fig. 10] having a device area and a thickness, the device area further including a plurality of contacts exposed on a bottom surface, a plurality of wire bonding landings [1-6] exposed on a top surface, lead segments[104] electrically coupling the wire bonding landings to associated lead contacts and a first dielectric layer [124] that fills spaces [122] between adjacent lead segments;

a die [130] mounted on the substrate, the die having a plurality of bond pads configured for electrical connection [through wire 140] to the wire bonding landings;

a plurality of connectors for electrically connecting the plurality of bond pads to associated wire bonding landings [col. 4, lines 31-32]; and

a second dielectric layer [a transparent material in the space 126; col. 4, lines 61-63] that encapsulates the die and the plurality of connectors.

Regarding claim 17, Fig. 5 of Huang shows an upper portion of the first dielectric layer is substantially coplanar with the top surface of the substrate and the plurality of wire bonding landings, and a lower portion of the first dielectric layer is substantially coplanar with the bottom surface of the substrate and the lead contacts.

Regarding claim 19, Fig. 5 of Huang shows at least selected portions of the lead segments are thinner than the thickness of the lead-frame, such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate.

Regarding claim 22, it is inherent that at least one of the wire bonding landings is electrically coupled to the die attach pad since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 6, 10, 16, 18, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Lee (US 6713322).

Regarding claim 3, fig. 5 of Huang shows the most aspect of the instant invention except "the wire bonding landings are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel." Fig. 8 of Lee shows a semiconductor device wherein "the wire bonding landings [10a, 10c] are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the wire

bonding landings thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel to improve the supporting structure of the package.

Regarding claim 6, Fig. 5 of Huang shows the most aspect of the instant invention except "the lead-frame further comprises a matrix of tie bars, the tie bars being positioned between adjacent device areas in the two dimensional array of device areas and configured to support the lead segments." Fig. 11 of Lee shows a semiconductor device wherein the lead-frame [100] further comprises a matrix of tie bars [4], the tie bars being positioned between adjacent device areas in the two dimensional array of device areas and configured to support the lead segments [col. 3, lines 34-37].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have a matrix of tie bars positioned between adjacent device areas in the two dimensional array of device areas and configured to support the lead segments for a secure package configuration.

Regarding claim 10, Fig. 5 of Huang shows the most aspect of the instant invention except "at least one of the contacts is located between the wire bonding landings and the die attach pad." Fig. 8 of Lee shows a semiconductor device wherein "at least one of the contacts [6] is located between the wire bonding landings [10] and the die attach pad [8].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have at least one of the contacts located between the wire bonding landings and the die attach pad to form a ground contact as taught by Lee.

Regarding claim 16, Fig. 5 of Huang shows the most aspect of the instant invention except "the first and second dielectric layers are formed from substantially the same materials." Fig. 10 of Lee shows a semiconductor device wherein the first and second dielectric layers are formed from substantially the same materials [26; a sealing material].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the first and second dielectric layers formed from substantially the same materials to reduce the processing steps.

The subject matter regarding claim 18 has been discussed in claim 3 above.

Regarding claim 20, Fig. 5 of Huang shows the most aspect of the instant invention except "a die attach pad surrounded by the lead contacts." Fig. 8 of Lee shows a semiconductor device wherein a die attach pad [8] surrounded by the lead contacts [6].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have to a die surrounded by the lead contacts to from a ground contact as taught by Lee.

The subject matter regarding claim 23 has been discussed in claim 10 above.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Chien-Hung et al. (US Pat. Pub. 2003/006055), hereinafter Chien-Hung.

Regarding claim 8, Fig. 5 of Huang shows the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel."

Fig. 1 of Chien-Hung shows a semiconductor wherein "the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate panel."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Chien-Hung in order to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate panel/a lead frame to improve the mounting capability to a circuit board.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Lee and Chien-Hung.

Regarding claim 13, Fig. 5 of Huang shows the most aspect of the instant invention except "the contacts surround the die attach pad, and wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the contacts and the posts being arranged in a two dimensional array." Fig. 8 of Lee shows a semiconductor device wherein the contacts [6] surround the die attach pad [8] while arranged in a two dimensional array.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the contacts located between the wire bonding landings and arranged in a two dimensional array to form a ground contact as taught by Lee.

The combined teachings of Huang and Lee shows the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the posts being arranged in a two dimensional array." Fig. 1 of Chien-Hung shows a

semiconductor wherein the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate panel and arranged in a two dimensional array.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Chien-Hung into the device of Huang and Lee in order to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate panel [a lead frame] and arranged in a two dimensional array to improve the mounting capability to a circuit board.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang and Lee as applied to claim 20 above, and further in view of Chien-Hung.

Regarding claim 21, the combined teachings of Huang and Lee show the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate." Fig. 1 of Chien-Hung shows a semiconductor wherein the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate/a lead frame.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Chien-Huang into the device of Huang and Lee in order to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate/a lead frame to improve the mounting capability to a circuit board.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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